APPENDIX B
Version With Markings To Show Changes Made
37 CFR 1.121(b)(iii) AND (c)(ii)

SPECIFICATION:

Paragraph at page 1, lines 2-3:

This is a division of application Serial No. 09/031,981, filed February 26, 1998, now U.S. Patent No. 6,445,255.

Paragraph at page 2, lines 4-18:

Meanwhile, since the distribution of electromagnetic field around input/output sections of electronic components, such as semiconductor devices, and the distribution of electromagnetic field around planar dielectric lines generally differ, merely mounting electronic component onto the planar dielectric line causes the conversion loss to increase greatly. Further, if electronic components are only mounted onto one surface of the [dialectric] dielectric plate, no connection is made between the electro magnetic field on the back surface thereof and the electronic components, this point also leading to an increase in the conversion loss. Mounting electronic components onto both surfaces of the dielectric plate eliminates the latter problem; however, this results in a decrease in the yield, an increase in loss, and an increase in the material and mounting costs.

Paragraph at page 13, line 6 to page 14, line 9:

Fig. 5 is a view showing the conductor patterns of the main portion of the top surface of the circuit substrate 30. In Fig. 5, reference numerals 12 and 13 each denote a slot line, which is formed in each of the end portions of two planar dielectric line. Reference numerals 10 and 11 each denote a line-conversion conductor pattern, which is formed in the shape of a dipole antenna, as indicated by 10a, 10b, 11a, and 11b,

respectively. [Another] Other shapes of the portions 10a, 10b, 11a and 11b are possible as long as the portions function as dipole antennas. The base portions of the line-conversion conductor patterns 10 and 11 form impedance matching sections R which are tapered moderately from the slot lines 12 and 13 toward the line-conversion conductor patterns 10 and 11 in order that the [writing] wiring resistance of the line-conversion conductor patterns 10 and 11 is reduced to decrease the conversion loss. If the wavelength of the frequency in the used frequency band in each of the electrode patterns 10a, 10b, 11a and 11b and the impedance matching section R is denoted as λ, they have a length of nearly $\lambda/4$, and the width of the slot lines 12 and 13 is determined by the characteristics impedance of the designed line. [When assuming] Assuming that Z_1 is the input impedance of a portion 100, Z_{01} is the impedance of a portion [11] L_1 and Z_{02} is the impedance of a portion [12] L_2, it is preferable that the relation of these values [are] is given by the following equation:

Paragraph at page 19, line 1 to page 20, line 7:

Fig. 7 is a perspective view in a state in which the circuit substrate 30 is placed on the lower conductor plate 44. This VCO is such that a resonator and a variable capacitive element are provided in the high-frequency amplifier shown in Fig. 1B. In Fig. 7, reference numeral 61 denotes a thin-film resistor, with the termination portion of the slot 14 formed on the top surface of the circuit substrate 30 being formed into a tapered shape and this thin-film resistor 61 being provided thereon. Reference numeral 74 denotes another slot provided on the top surface of the circuit substrate 30 and, as will be described later, a slot is also provided on the back-surface side of the circuit substrate 30 with the circuit substrate 30 interposed in between, forming the planar dielectric line. Reference numeral 60 denotes a variable capacitive element mounted in such a manner as to be extended over a slot 74, whose capacitance varies according to an applied voltage. As this variable capacitive element, a variable capacitive capacitor disclosed in Japanese Unexamined Patent Publication No. 5-74655, and a conventional variable capacitive diode

APPENDIX C
"Clean" Version Without Amended/New Indications
37 CFR 1.121(c)(3)

5. A planar dielectric integrated circuit, comprising:

a first planar dielectric line comprising: a first slot which is provided by disposing two conductors at a fixed distance apart on a first main surface of a dielectric plate, and a second slot, which opposes the first slot and is provided by disposing two conductors at a fixed distance apart on a second main surface of said dielectric plate, with a region sandwiched between said first slot and said second slot being provided as a plane-wave propagation region;

a dielectric resonator provided by a pair of mutually opposing conductor-free portions within corresponding ones of said conductors on said first and second main surfaces of said dielectric plate, said dielectric resonator being electromagnetically coupled to said first planar dielectric line;

a slot line provided at an end portion of said first planar dielectric line on said dielectric plate;

line conversion conductor patterns which are connected to said first planar dielectric line and which are used to perform mode conversion between said first planar dielectric line and said slot line; and

electronic components disposed in such a manner as to be extended over said slot line.

6. The circuit of claim 5, further comprising:

a second planar dielectric line comprising: a third slot which is provided by disposing two conductors at a fixed distance apart on said first main surface of said dielectric plate, and a fourth slot, which opposes the third slot and is provided by disposing two conductors at a fixed distance apart on said second main surface of said dielectric plate,

with a region sandwiched between said third slot and said fourth slot being provided as a plane-wave propagation region;

said second planar dielectric line being electromagnetically coupled to said dielectric resonator.

7. The circuit of claim 6, wherein said dielectric resonator is coupled to an end of said second planar dielectric line.

8. A planar dielectric integrated circuit, comprising:

a first planar dielectric line comprising: a first slot which is provided by disposing two conductors at a fixed distance apart on a first main surface of a dielectric plate, and a second slot, which opposes the first slot and is provided by disposing two conductors at a fixed distance apart on a second main surface of said dielectric plate, with a region sandwiched between said first slot and said second slot being provided as a plane-wave propagation region;

a slot line provided at an end portion of said first planar dielectric line on said dielectric plate;

line-conversion conductor patterns which are connected to said first planar dielectric line and which are used to perform mode conversion between said first planar dielectric line and said slot line; and

electronic components disposed in such a manner as to be extended over said slot line.

9. The circuit of claim 5, further comprising:

a conductive plate adjacent at least one of the first and second main surfaces of the dielectric plate, the conductive plate having at least one groove in a surface thereof, the at least one groove opposing at least one of the first planar dielectric line, the slot line and the line-conversion conductor patterns.

10. The circuit according to claim 9, wherein a width of the at least one groove is greater than a width of the first planar dielectric line.

11. The circuit according to claim 10, wherein the width of the at least one groove is set such that a cut-off area is formed, the cut-off area having a propagation frequency which is higher than a desired propagation frequency of the plane-wave propagation region.

12. The circuit according to claim 11, wherein a depth of the at least one groove is set such that a cut-off area is formed, the cut-off area having a propagation frequency which is higher than a desired propagation frequency of the plane-wave propagation region.

13. The circuit according to claim 6, further comprising:

at least one conductive plate adjacent one of the first and second main surfaces of the dielectric plate, the conductive plate having at least one groove in a surface thereof, the at least one groove opposing at least one of the first planar dielectric line, the slot line, the line-conversion conductor patterns, and the second planar dielectric line.

14. The circuit according to claim 13, wherein a width of the at least one groove is greater than a width of one of the first planar dielectric line and the second planar dielectric line.

15. The circuit according to claim 14, wherein the width of the at least one groove is set such that a cut-off area is formed, the cut-off area having a propagation frequency which is higher than a desired propagation frequency of the plane-wave propagation region.

16. The circuit according to claim 15, wherein a depth of the at least one groove is set such that a cut-off area is formed, the cut-off area having a propagation

frequency which is higher than a desired propagation frequency of the plane-wave propagation region.

17. The circuit of claim 8, further comprising:

a conductive plate adjacent at least one of the first and second main surfaces of the dielectric plate, the conductive plate having at least one groove in a surface thereof, the at least one groove opposing at least one of the first planar dielectric line, the slot line and the line-conversion conductor patterns.

18. The circuit according to claim 17, wherein a width of the at least one groove is greater than a width of the first planar dielectric line.

19. The circuit according to claim 18, wherein the width of the at least one groove is set such that a cut-off area is formed, the cut-off area having a propagation frequency which is higher than a desired propagation frequency of the plane-wave propagation region.

20. The circuit according to claim 19, wherein a depth of the at least one groove is set such that a cut-off area is formed, the cut-off area having a propagation frequency which is higher than a desired propagation frequency of the plane-wave propagation region.